

**ADG619/ADG620**
**FEATURES**

**6  $\Omega$  (Max) On Resistance**  
**0.8  $\Omega$  (Max) On-Resistance Flatness**  
**2.7 V to 5.5 V Single Supply**  
 **$\pm 2.7$  V to  $\pm 5.5$  V Dual Supply**  
**Rail-to-Rail Operation**  
**8-Lead SOT-23 Package, 8-Lead Micro-SOIC Package**  
**Typical Power Consumption (<0.1  $\mu$ W)**  
**TTL/CMOS Compatible Inputs**

**APPLICATIONS**

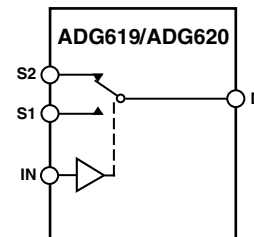
**Automatic Test Equipment**  
**Power Routing**  
**Communication Systems**  
**Data Acquisition Systems**  
**Sample and Hold Systems**  
**Avionics**  
**Relay Replacement**  
**Battery-Powered Systems**

**GENERAL DESCRIPTION**

The ADG619 and the ADG620 are monolithic, CMOS SPDT (single pole, double throw) switches. Each switch conducts equally well in both directions when on.

The ADG619/ADG620 offers low On-Resistance of 4  $\Omega$ , which is matched to within 0.7  $\Omega$  between channels. These switches also provide low power dissipation yet give high switching speeds. The ADG619 exhibits break-before-make switching action, thus preventing momentary shorting when switching channels. The ADG620 exhibits make-before-break action.

The ADG619/ADG620 are available in 8-lead SOT-23 packages and 8-lead Micro-SOIC packages.

**FUNCTIONAL BLOCK DIAGRAM**


SWITCHES SHOWN FOR A LOGIC "1" INPUT

**Table I. Truth Table for the ADG619/ADG620**

IN	Switch S1	Switch S2
0	ON	OFF
1	OFF	ON

**PRODUCT HIGHLIGHTS**

1. Low On Resistance ( $R_{ON}$ ) (4  $\Omega$  typ)
2. Dual  $\pm 2.7$  V to  $\pm 5.5$  V or Single 2.7 V to 5.5 V
3. Low Power Dissipation. CMOS construction ensures low power dissipation.
4. Fast  $t_{ON}/t_{OFF}$
5. Tiny 8-Lead SOT-23 Package and 8-Lead Micro-SOIC Package

REV. 0

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices.

# ADG619/ADG620—SPECIFICATIONS

**DUAL SUPPLY<sup>1</sup>** ( $V_{DD} = +5\text{ V} \pm 10\%$ ,  $V_{SS} = -5\text{ V} \pm 10\%$ ,  $GND = 0\text{ V}$ . All specifications  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$  unless otherwise noted.)

Parameter	B Version -40°C to +85°C		Unit	Test Conditions/Comments
	+25°C			
<b>ANALOG SWITCH</b>				
Analogue Signal Range		$V_{SS}$ to $V_{DD}$	V	$V_{DD} = +4.5\text{ V}$ , $V_{SS} = -4.5\text{ V}$
On Resistance ( $R_{ON}$ )	4 6	8	$\Omega$ typ $\Omega$ max	$V_S = \pm 4.5\text{ V}$ , $I_S = -10\text{ mA}$ , Test Circuit 1
On Resistance Match Between Channels ( $\Delta R_{ON}$ )	0.7 1.1	1.35	$\Omega$ typ $\Omega$ max	$V_S = \pm 4.5\text{ V}$ , $I_S = -10\text{ mA}$
On-Resistance Flatness ( $R_{FLAT(ON)}$ )	0.7	0.8 1.2	$\Omega$ typ $\Omega$ max	$V_S = \pm 3.3\text{ V}$ , $I_S = -10\text{ mA}$
<b>LEAKAGE CURRENTS</b>				
Source OFF Leakage $I_S$ (OFF)	$\pm 0.01$ $\pm 0.25$	$\pm 1$	nA typ nA max	$V_{DD} = +5.5\text{ V}$ , $V_{SS} = -5.5\text{ V}$ $V_S = \pm 4.5\text{ V}$ , $V_D = \mp 4.5\text{ V}$ , Test Circuit 2
Channel ON Leakage $I_D$ , $I_S$ (ON)	$\pm 0.01$ $\pm 0.25$	$\pm 1$	nA typ nA max	$V_S = V_D = \pm 4.5\text{ V}$ , Test Circuit 3
<b>DIGITAL INPUTS</b>				
Input High Voltage, $V_{INH}$		2.4	V min	
Input Low Voltage, $V_{INL}$		0.8	V max	
Input Current $I_{INL}$ or $I_{INH}$	0.005	$\pm 0.1$	$\mu\text{A}$ typ $\mu\text{A}$ max	$V_{IN} = V_{INL}$ or $V_{INH}$
$C_{IN}$ , Digital Input Capacitance	2		pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>2</sup></b>				
<b>ADG619</b>				
$t_{ON}$	80 120	155	ns typ ns max	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ $V_S = 3.3\text{ V}$ , Test Circuit 4
$t_{OFF}$	45 75	90	ns typ ns max	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ $V_S = 3.3\text{ V}$ , Test Circuit 4
Break-Before-Make Time Delay, $t_{BBM}$	40	10	ns typ ns min	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ $V_{S1} = V_{S2} = 3.3\text{ V}$ , Test Circuit 5
<b>ADG620</b>				
$t_{ON}$	40 65	85	ns typ ns max	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ $V_S = 3.3\text{ V}$ , Test Circuit 4
$t_{OFF}$	200 330	400	ns typ ns max	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ $V_S = 3.3\text{ V}$ , Test Circuit 4
Make-Before-Break Time Delay, $t_{MBB}$	160	10	ns typ ns min	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ $V_S = 0\text{ V}$ , Test Circuit 6
Charge Injection	110		pC typ	$V_S = 0\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ , Test Circuit 7
Off Isolation	-67		dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ , Test Circuit 8
Channel-to-Channel Crosstalk	-67		dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ , Test Circuit 10
Bandwidth -3 dB	190		MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , Test Circuit 9
$C_S$ (OFF)	25		pF typ	$f = 1\text{ MHz}$
$C_D$ , $C_S$ (ON)	95		pF typ	$f = 1\text{ MHz}$
<b>POWER REQUIREMENTS</b>				
$I_{DD}$	0.001	1.0	$\mu\text{A}$ typ $\mu\text{A}$ max	$V_{DD} = +5.5\text{ V}$ , $V_{SS} = -5.5\text{ V}$ Digital Inputs = 0 V or 5.5 V
$I_{SS}$	0.001	1.0	$\mu\text{A}$ typ $\mu\text{A}$ max	Digital Inputs = 0 V or 5.5 V

## NOTES

<sup>1</sup>Temperature ranges are as follows: B Version,  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

<sup>2</sup>Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

**SINGLE SUPPLY<sup>1</sup>** ( $V_{DD} = +5\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $GND = 0\text{ V}$ . All specifications  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  unless otherwise noted.)

Parameter	B Version		Unit	Test Conditions/Comments
	+25°C	-40°C to +85°C		
<b>ANALOG SWITCH</b>				
Analog Signal Range		0 V to $V_{DD}$	V	$V_{DD} = 4.5\text{ V}$ , $V_{SS} = 0\text{ V}$
On Resistance ( $R_{ON}$ )	7		$\Omega$ typ	$V_S = 0\text{ V}$ to 4.5 V, $I_S = -10\text{ mA}$ , Test Circuit 1
	$\beta 10$	12.5	$\Omega$ max	
On Resistance Match Between Channels ( $\Delta R_{ON}$ )	0.8		$\Omega$ typ	$V_S = 0\text{ V}$ to 4.5 V, $I_S = -10\text{ mA}$
	1	1.2	$\Omega$ max	
On-Resistance Flatness ( $R_{FLAT(ON)}$ )	0.5	0.5	$\Omega$ typ	$V_S = 1.5\text{ V}$ to 3.3 V, $I_S = -10\text{ mA}$
		0.8	$\Omega$ max	
<b>LEAKAGE CURRENTS</b>				
Source OFF Leakage $I_S$ (OFF)	$\pm 0.01$		nA typ	$V_{DD} = 5.5\text{ V}$ $V_S = 1\text{ V}/4.5\text{ V}$ , $V_D = 4.5\text{ V}/1\text{ V}$ , Test Circuit 2
	$\pm 0.25$	$\pm 1$	nA max	
Channel ON Leakage $I_D$ , $I_S$ (ON)	$\pm 0.01$		nA typ	$V_S = V_D = 1\text{ V}/4.5\text{ V}$ , Test Circuit 3
	$\pm 0.25$	$\pm 1$	nA max	
<b>DIGITAL INPUTS</b>				
Input High Voltage, $V_{INH}$		2.4	V min	
Input Low Voltage, $V_{INL}$		0.8	V max	
Input Current $I_{INL}$ or $I_{INH}$	0.005		$\mu\text{A}$ typ	$V_{IN} = V_{INL}$ or $V_{INH}$
		$\pm 0.1$	$\mu\text{A}$ max	
$C_{IN}$ , Digital Input Capacitance	2		pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>2</sup></b>				
<b>ADG619</b>				
$t_{ON}$	120		ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	220	280	ns max	$V_S = 3.3\text{ V}$ , Test Circuit 4
$t_{OFF}$	50		ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	75	110	ns max	$V_S = 3.3\text{ V}$ , Test Circuit 4
Break-Before-Make Time Delay, $t_{BBM}$	70		ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ , $V_{S1} = V_{S2} = 3.3\text{ V}$ , Test Circuit 5
		10	ns min	
<b>ADG620</b>				
$t_{ON}$	50		ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	85	110	ns max	$V_S = 3.3\text{ V}$ , Test Circuit 4
$t_{OFF}$	210		ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
	340	420	ns max	$V_S = 3.3\text{ V}$ , Test Circuit 4
Make-Before-Break Time Delay, $t_{MBB}$	170		ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$
		10	ns min	$V_S = 3.3\text{ V}$ , Test Circuit 6
Charge Injection	6		pC typ	$V_S = 0\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ , Test Circuit 7
Off Isolation	-67		dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ , Test Circuit 8
Channel-to-Channel Crosstalk	-67		dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ , Test Circuit 10
Bandwidth -3 dB	190		MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , Test Circuit 9
$C_S$ (OFF)	25		pF typ	$f = 1\text{ MHz}$
$C_D$ , $C_S$ (ON)	95		pF typ	$f = 1\text{ MHz}$
<b>POWER REQUIREMENTS</b>				
$I_{DD}$	0.001		$\mu\text{A}$ typ	$V_{DD} = 5.5\text{ V}$ Digital Inputs = 0 V or 5.5 V
		1.0	$\mu\text{A}$ max	

## NOTES

<sup>1</sup>Temperature ranges are as follows: B Version,  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .<sup>2</sup>Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

# ADG619/ADG620

## ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

(T<sub>A</sub> = 25°C unless otherwise noted)

V <sub>DD</sub> to V <sub>SS</sub> .....	13 V
V <sub>DD</sub> to GND .....	-0.3 V to +6.5 V
V <sub>SS</sub> to GND .....	+0.3 V to -6.5 V
Analog Inputs <sup>2</sup> .....	V <sub>SS</sub> -0.3 V to V <sub>DD</sub> +0.3 V
Digital Inputs <sup>2</sup> .....	-0.3 V to V <sub>DD</sub> +0.3 V or 30 mA, Whichever Occurs First
Peak Current, S or D .....	100 mA (Pulsed at 1 ms, 10% Duty Cycle max)
Continuous Current, S or D .....	50 mA
Operating Temperature Range	
Industrial (B Version) .....	-40°C to +85°C
Storage Temperature Range .....	-65°C to +150°C
Junction Temperature .....	150°C
Micro-SOIC Package	
θ <sub>JA</sub> Thermal Impedance .....	206°C/W
θ <sub>JC</sub> Thermal Impedance .....	44°C/W
SOT-23 Package	
θ <sub>JA</sub> Thermal Impedance .....	229.6°C/W
θ <sub>JC</sub> Thermal Impedance .....	91.99°C/W
Lead Temperature, Soldering (10 seconds) .....	300°C
IR Reflow, Peak Temperature .....	220°C

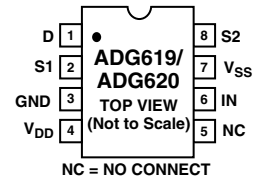
## NOTES

<sup>1</sup>Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

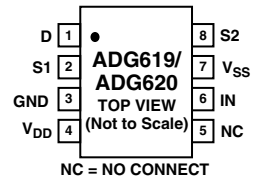
<sup>2</sup>Overvoltages at IN, S or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

## PIN CONFIGURATIONS

### 8-Lead SOT-23 (RT-8)



### 8-Lead Micro-SOIC (RM-8)



## ORDERING GUIDE

Model	Temperature Range	Branding Information*	Package Description	Package Option
ADG619BRM	-40°C to +85°C	SVB	Micro-SOIC (microSmall Outline IC)	RM-8
ADG619BRT	-40°C to +85°C	SVB	SOT-23 (Plastic Surface Mount)	RT-8
ADG620BRM	-40°C to +85°C	SWB	Micro-SOIC (microSmall Outline IC)	RM-8
ADG620BRT	-40°C to +85°C	SWB	SOT-23 (Plastic Surface Mount)	RT-8

\*Branding on SOT-23 and Micro-SOIC packages is limited to three characters due to space constraints.

## CAUTION

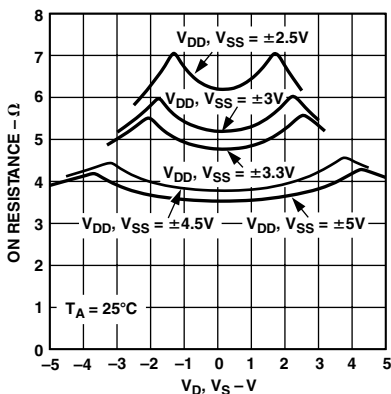
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG619/ADG620 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



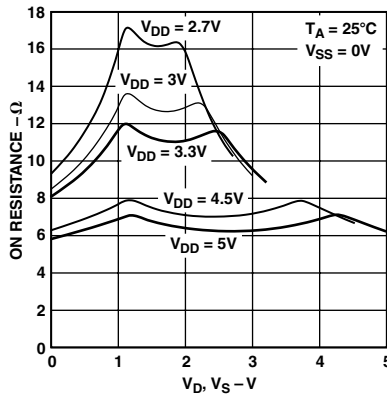
TERMINOLOGY

Mnemonic	Description
$V_{DD}$	Most Positive Power Supply Potential
$V_{SS}$	Most Negative Power Supply in a Dual Supply Application. In single supply applications, this should be tied to ground at the device.
GND	Ground (0 V) Reference
$I_{DD}$	Positive Supply Current
$I_{SS}$	Negative Supply Current
S	Source Terminal. May be an input or output.
D	Drain Terminal. May be an input or output.
IN	Logic Control Input
$R_{ON}$	Ohmic Resistance Between D and S
$DR_{ON}$	On Resistance Match Between Any Two Channels, i.e., $R_{ON} \text{ Max} - R_{ON} \text{ Min}$ .
$R_{FLAT(ON)}$	Flatness is Defined as the Difference Between the Maximum and Minimum Value of On Resistance as Measured Over the Specified Analog Signal Range.
$I_S$ (OFF)	Source Leakage Current With the Switch "OFF"
$I_D, I_S$ (ON)	Channel Leakage Current With the Switch "ON"
$V_D$ ( $V_S$ )	Analog Voltage on Terminals D, S
$V_{INL}$	Maximum Input Voltage for Logic "0"
$V_{INH}$	Minimum Input Voltage for Logic "1"
$I_{INL}$ ( $I_{INH}$ )	Input Current of the Digital Input
$C_S$ (OFF)	"OFF" Switch Source Capacitance
$C_D, C_S$ (ON)	"ON" Switch Capacitance
$t_{ON}$	Delay Between Applying the Digital Control Input and the Output Switching On
$t_{OFF}$	Delay Between Applying the Digital Control Input and the Output Switching Off
$t_{MBS}$	"ON" Time, Measured Between the 80% Points of Both Switches, When Switching From One Address State to Another
$t_{BBS}$	"OFF" Time or "ON" Time Measured Between the 90% Points of Both Switches, When Switching from One Address State to Another
Charge Injection	A Measure of the Glitch Impulse Transferred From the Digital Input to the Analog Output During Switching
Crosstalk	A Measure of Unwanted Signal that is Coupled Through From One Channel to Another as a Result of Parasitic Capacitance
Off Isolation	A Measure of Unwanted Signal Coupling Through an "OFF" Switch
Bandwidth	The Frequency Response of the "ON" Switch
Insertion Loss	The Loss Due to the ON Resistance of the Switch

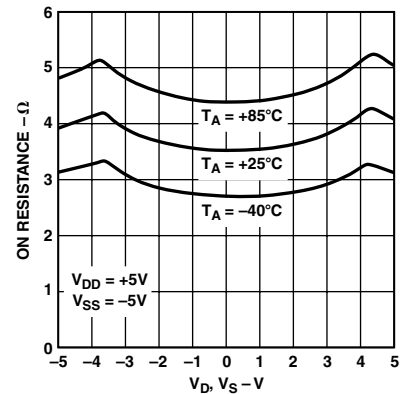
Typical Performance Characteristics



TPC 1. On Resistance vs.  $V_D$  ( $V_S$ ) – Dual Supply

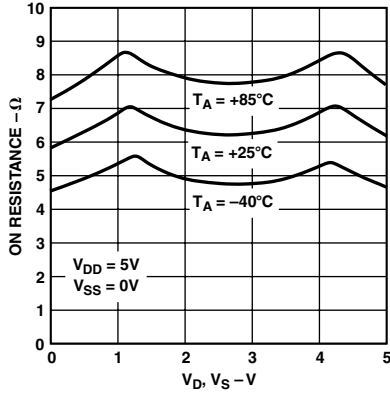


TPC 2. On Resistance vs.  $V_D$  ( $V_S$ ) – Single Supply

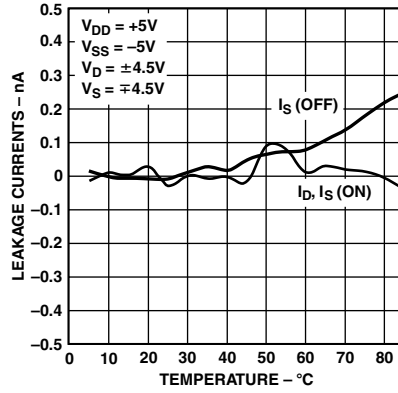


TPC 3. On Resistance vs.  $V_D$  ( $V_S$ ) for Different Temperatures – Dual Supply

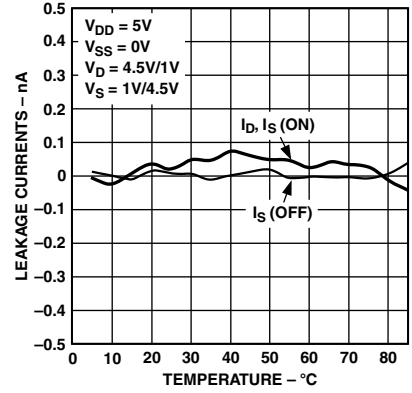
# ADG619/ADG620—Typical Performance Characteristics



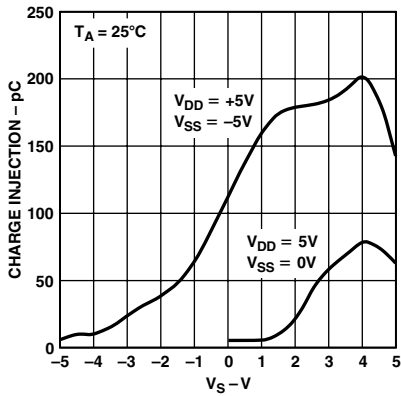
TPC 4. On Resistance vs.  $V_D$  ( $V_S$ ) for Different Temperatures – Single Supply



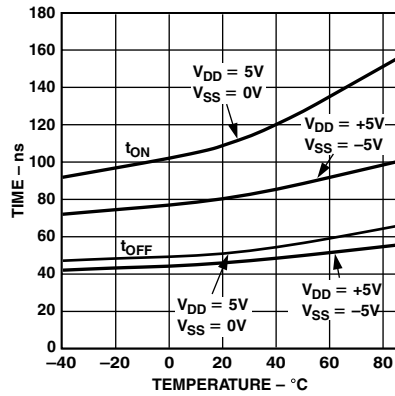
TPC 5. Leakage Currents vs. Temperature – Dual Supply



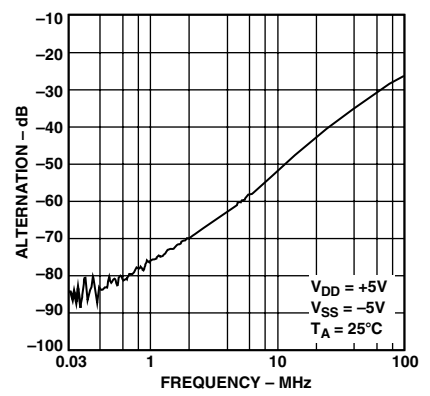
TPC 6. Leakage Currents vs. Temperature – Single Supply



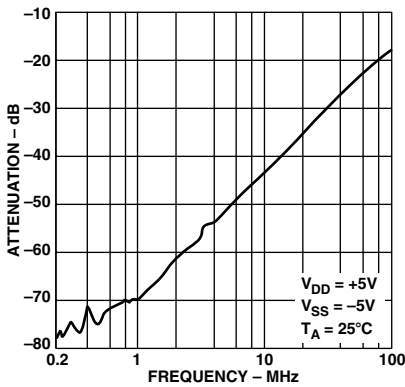
TPC 7. Charge Injection vs. Source Voltage



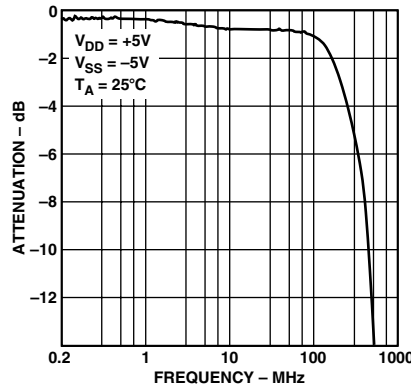
TPC 8.  $t_{ON}/t_{OFF}$  Times vs. Temperature



TPC 9. Off Isolation vs. Frequency

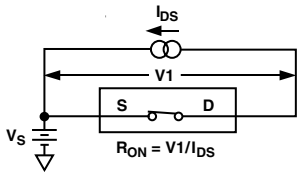


TPC 10. Crosstalk vs. Frequency

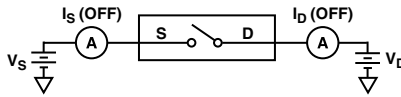


TPC 11. On Response vs. Frequency

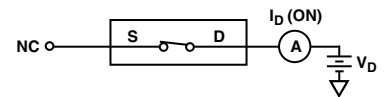
## TEST CIRCUITS



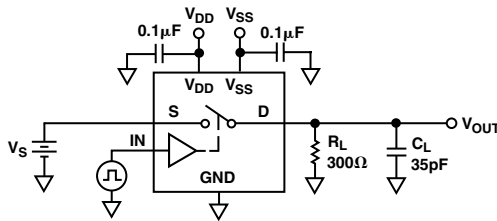
Test Circuit 1. On Resistance



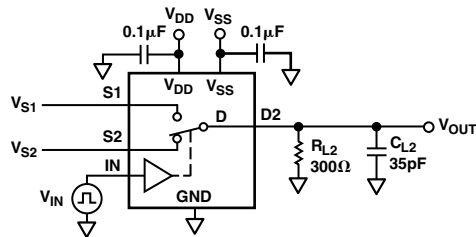
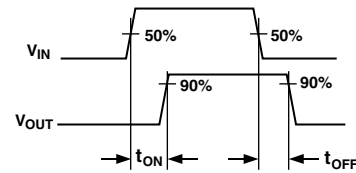
Test Circuit 2. Off Leakage



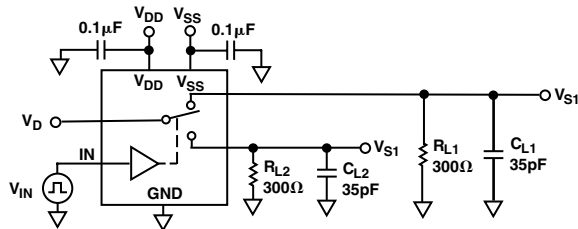
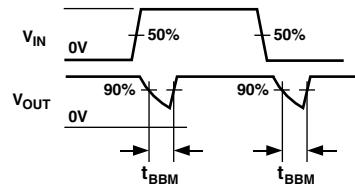
Test Circuit 3. On Leakage



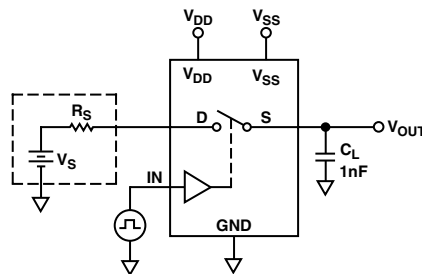
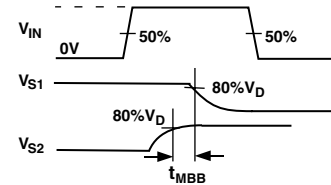
Test Circuit 4. Switching Times



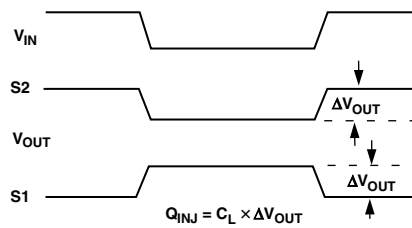
Test Circuit 5. Break-Before-Make Time Delay,  $t_{BBM}$  (ADG619 Only)



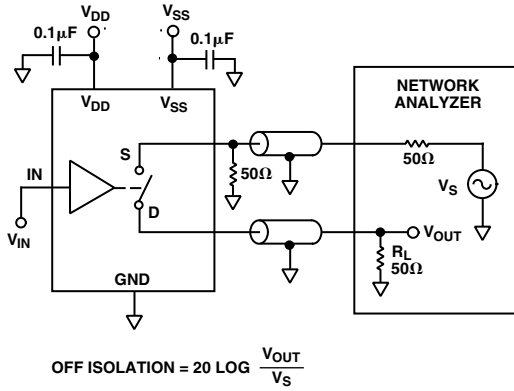
Test Circuit 6. Make-Before-Break Time Delay,  $t_{MBB}$  (ADG620 Only)



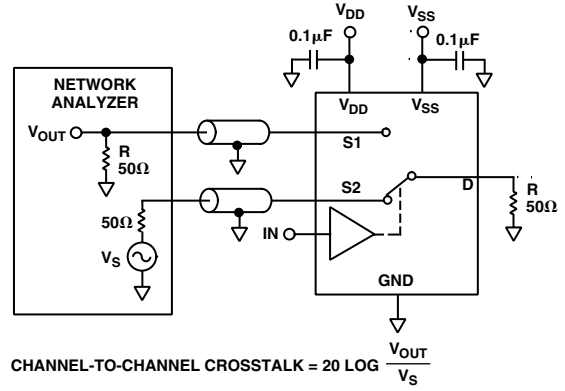
Test Circuit 7. Charge Injection



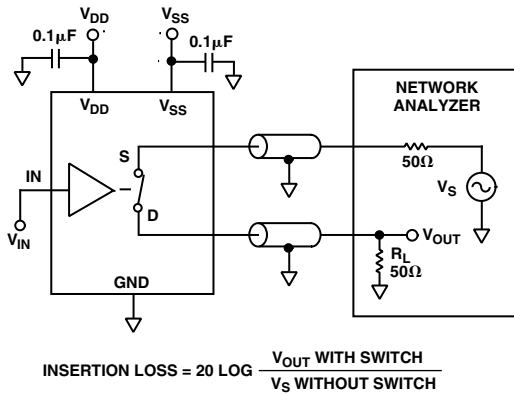
# ADG619/ADG620



Test Circuit 8. Off Isolation



Test Circuit 10. Channel-to-Channel Crosstalk

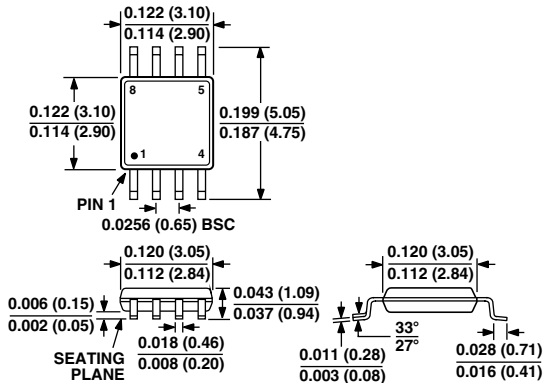


Test Circuit 9. Bandwidth

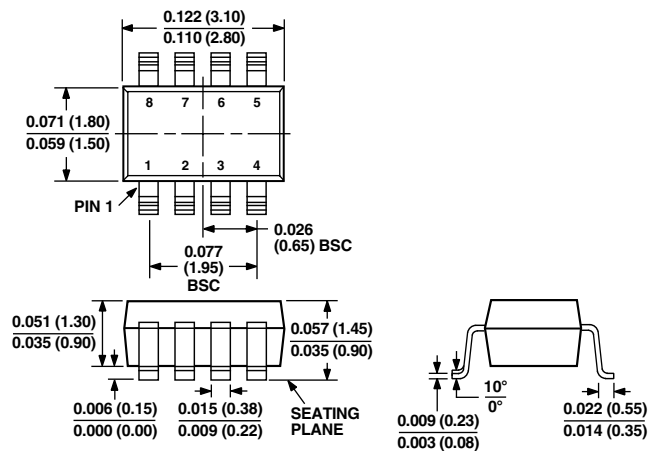
## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

### 8-Lead Micro-SOIC Package (RM-8)



### 8-Lead Plastic Surface Mount Package (RT-8)



C02617-8-10/01(0)

PRINTED IN U.S.A.